



6-7-04
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

2133
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Applicants: Christopher H. Pham

Assignee: Cisco Technology, Inc.

Title: LINEAR ASSOCIATIVE MEMORY-BASED HARDWARE
ARCHITECTURE FOR FAULT TOLERANT ASIC/FPGA
WORKAROUND

Serial No.: 09/837,882

Filed: April 18, 2001

Examiner: Unassigned

Group Art Unit: 2133

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Austin, Texas
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**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(b)**

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying PTO Form-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

EXPRESS MAIL NUMBER:

EV 304738815 US

Respectfully submitted,

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